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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
JORGENSEN, LELAND R

ART UNIT	PAPER NUMBER
2675	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/492,789	YANO ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 31 December 2003 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/492,789 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Objections

2. Claim 13 is objected to because of the following informalities: Claim 13 is dependent on claim 1 and adds that the amplifying elements are operational amplifiers. Claim 1 does not describe operational amplifiers. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5 and 6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 5 (amended) adds that 'the number of diodes of the diode group is determined from the sum of the voltage drop of each diode being approximately equal to the data driver

voltage." Nothing in the specification describes this limitation. In fact, the specification says that the sum of the voltage drop of each diode when the number of diodes is seven is 4.2 volts and that the data driver voltage is 3.6 volts. Specification, page 9, lines 34 – page 10, lines 11. Claim 6 (amended) adds that the "number of diodes of the diode group is seven."

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4 – 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 (amended) describes a diode group including a plurality of series-connected diodes "wherein the series-connected diodes each have a cathode terminal connected to the control terminal of the amplifying element, and an anode terminal connected to the ground respectfully." As written, this suggests that each diode has a cathode terminal connected to the control terminal of the amplifying element, and an anode terminal connected to the ground. This would be a parallel rather than a series-connected diodes. As described in the specification, the group consists of a series of diodes with the first diode having a cathode terminal connected to the control terminal of the amplifying element, the subsequent diodes in series with the first diode with cathode terminal connected to the anode terminal of the prior diode and the anode of the final diode connected to ground. See specification, figure 3A.

Claims 5 and 6 are further rejected as dependant on indefinite claim 4.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 6, 9 – 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al., USPN 5,663,743, in view of Sakamoto et al., USPN 3,956,661.

Claim 1 (twice amended)

Claim 1 (twice amended) describes a power supply circuit. Fujii teaches a scan power supply circuit to supply scan drive voltage to a scan driver for scanning a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 22 – 24, 29 – 36; and figures 1 and 2. Fujii teaches a data power supply circuit to supply data drive voltage to a data driver for sending display data to a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 17, 29 – 36; and figures 1 and 2.

Claim 1 (twice amended) describes a brightness control circuit, provided in the scan driver power circuit, for controlling brightness of the liquid crystal display device by changing the voltage level of the scan driver voltage. The specification states, "With this constitution, when a user changes the base voltage of the transistor 126 by manipulating the variable resistor 124, the scan drive voltage 132 stably varies in response thereto." Specification, page 11, lines 2 – 5. See Specification, figure 3B. Fujii teaches a variable resistor R1 that allows the user to change the base voltage of a transistor Tr, thus varying the scan voltage V_2. Fujii, col. 6, lines 4 – 15; and figure 1.

Claim 1 (twice amended) describes a voltage regulation circuit, provided in the data driver power circuit, for regulating the voltage level of the data driver voltage supplied to the liquid crystal display device to a predetermined value; and a temperature compensation circuit, provided in the data driver power circuit, for compensating a temperature characteristic of the liquid crystal display device by changing the voltage level of the data driver voltage.

Fujii does not teach a voltage regulation circuit and temperature compensation circuit.

Sakamoto teaches a voltage regulation circuit and temperature compensation circuit.. Sakamoto, figure 1; col. 2, lines 22 – 33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the voltage regulation and temperature compensation circuit of Sakamoto with the data drive power circuit of Fujii to create a temperature compensation data drive power circuit. Sakamoto invite such combination by teaching,

> The present invention relates to an improved D.C. power source for stabilizing an output voltage and/or current especially in integrated circuits (IC) and also for compensating for deviation or fluctuation in the current amplification factor h_{FE} or β of a transistor due to variation in the ambient temperature.
>
> Heretofore, in a transistor circuit for supplying constant output voltage, a power supply voltage was divided by a pair of bias resistors including an emitter resistor in a transistor circuit built in an integrated circuit block, and the divided voltage was supplied to a transistor or transistors also built in the integrated circuit blocks. However, in a prior D.C. power source the compensation for preventing the change of the output voltage due to temperature change was not enough because the values of the resistances in the IC blocks were considerably varied by discrepancies among resistors as well as temperature variations, and it was very difficult to construct a transistor circuit in which an absolute value of the current flowing through a load was maintained constant.

Sakamoto et al., col. 1, lines 5 – 10. Sakamoto adds,

> A main purpose of the present invention is, therefore, to provide a D.C. power source having a temperature compensation circuit in which variation in the

> voltage drop between the base and emitter of a transistor due to variation in the ambient temperature is compensated.
>
> Another purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which variation or deviation of the current amplification factor h_{FE} or β due to variation in the ambient temperature is compensated.
>
> A still further purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which the effect of variation in the ambient temperature on the output voltage and/or current compensated.

Sakamoto, col. 1, lines 29 – 45.

Claim 2 (amended)

Fujii teaches that the data driver power circuit includes input power supply V_{CC} serving as a universal power supply. Fujii, figure 1; col. 5, lines 29 – 36; and col. 6, lines 4 – 8. Sakamoto also shows an input power supply, V_{cc}. Sakamoto, figure 2.

Claim 2 (amended) describes an amplifying element with an input terminal connected to the input power supply, a control terminal, and an output terminal from which the data power driver power voltage is outputted. The specification gives an example of an amplifying device being a bipolar transistor with the collector being the input terminal, the base being the control terminal, and the emitter being the output terminal. Fujii shows a transistor Tr with a collector, base, and emitter. Fujii, figure 1; and col. 6, lines 4 - 12. Sakamoto also teaches an amplifying element, showing a transistor 1 with a collector, base, and emitter. Sakamoto, figure 2; col. 2, lines 22 – 33.

Claim 2 (amended) describes an impedance element connected between the input power circuit and the control terminal of the amplifying element. Fujii shows a variable resister R1 that has a portion of the resistance between the input power supply and the control terminal of the

amplifying element. Fujii, figure 1; and col. 6, lines 4 – 11. Sakamoto also shows a resister R1 connected between the input power supply and the control terminal of the amplifying element. Sakamoto, figure 2; col. 2, lines 22 – 33.

Sakamoto shows the voltage regulation circuit and the temperature compensation circuit connected to the control terminal of the amplifying element. Sakamoto, figure 2.

Claim 3 (amended)

Sakamoto teaches that the voltage regulation circuit and the temperature compensation circuit comprise a diode group having a plurality of series connected diodes connected between the control terminal of the amplifying element and ground. Sakamoto, figure 1; col. 2, lines 22 – 33.

Claim 4 (amended)

Sakamoto teaches that the series-connected diodes with a first diode having a cathode terminal connected to the control terminal of the amplifying element and a second diode with an anode terminal connected to the ground respectively. Sakamoto, figure 1; col. 2, lines 22 – 33.

Claim 5 (amended)

Sakamoto teaches a circuit where the sum of the voltage drop of each diode, the voltage V_{B1} at the junction point (a), is equal to the data driver voltage V_{E1}. Sakamoto, col. 4, lines 2 – 6.

Claim 6 (amended)

Claim 6 (Amended) adds that the number of diodes of the diode group is seven.

Sakamoto does not specify the number of diodes as seven.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use seven diodes in the diode group. Sakamoto invites one to vary the number of diode. After defining *m* as the number of diode between the control terminal and ground, Sakamoto states,

> As described above, whenever the dividing ration of the D.C. power supply voltage V_{CC} is desired, the first and second resisters R1 and R2 and values of *m* and *n* are in turn determined. Thus the effect of the change of the voltage drop between the base and emitter V_{BE} of the transistor 1 due to temperature change is completely avoided by inserting a predetermined number of diodes 6.

Sakamoto, col. 3, lines 17 – 24. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain number of diodes to set an appropriate voltage drop.

Claim 9 (amended)

Sakamoto teaches that the amplifying elements are transistors. Sakamoto, figure 2, col. 2, lines 22 – 33. Although Sakamoto does not specifically state in the specifications that the transistors are bipolar, bipolar transistors would be inherent because the symbol of the transistor used in Sakamoto's figures are those typically used for bipolar transistors.

Claim 10 (amended)

Claim 10 (Amended) adds that the resistance of the current limiting resister is within a range of 40 kΩ to 50 kΩ.

Sakamoto does not specify the resistance of the current limiting resistor within a range of 40 kΩ to 50 kΩ.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a range. Sakamoto invites one to consider different resistances. Sakamoto, col. 3, lines 17 – 24. Sakamoto offers formulas to find such resistances. Sakamoto, col. 2, line 21 –

col. 3, line 32. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain resistance to produce an appropriate current.

Claim 11 (amended)

Claim 11 (amended) adds that the diodes of the diode group are silicon diodes.

Sakamoto does not specifically describe the diodes as silicon.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon diodes for the diodes of the diode group. Silicon diodes are readily available and well know in the art, as admitted in applicant's specification, page 2, lines 11 – 12.

Claim 18

Fujii teaches a voltage regulation function and a power supply function for the liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 24, 29 – 36; and figures 1 and 2. Sakamoto teaches a temperature compensation function. Sakamoto, col. 1, lines 5 – 10, 29 – 55. It is inherent that the data driver power circuit described by Fujii and Sakamoto would perform these functions at the same time.

9. Claims 7, 8, and 14 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., and Fujii et al., as applied to claim 1 above, and further in view of Nishioka, et al., USPN 6,121,943.

Claim 7 (amended)

Claim 7 (Amended) adds details of the scan driver power circuit.

Fujii teaches input power supply V_{CC} serving as a universal power supply. Fujii, figure 1; col. 5, lines 29 – 36; and col. 6, lines 4 – 8. Nishioka also teaches a power supply 80. Nishioka, figures 4 and 6, col. 5, lines 51 – 55.

Fujii teaches an amplifying element for the data driver power supply with the input terminal connection to the input power supply and different amplifying elements for the scan driver power supply. The terminal connections for the amplifying element for the scan power supply, however, do not track the terminal connections of claim 2. Fujii, figure 1.

Nishioka teaches a amplifying element 81a with an input power supply, control terminal, and output terminal from which the data power driver voltage is outputted. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

Claim 2 describes a divider circuit between the input power supply and ground. The divider circuit sets an upper value of a voltage applied to the control terminal of the amplifying element of the scan driver power circuit.

Sakamoto and Fujii do not teach such divider circuit.

Nishioka teaches such divider circuit. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. See discussion in claim 3 below. a divider circuit, provided between the input power supply and the ground, for setting a voltage applied to the control terminal of the amplifying element; and

Claim 2 describes a variable resister having a resistance variation terminal connected to the control terminal of the amplifying element. The variable resistors allows the voltage at the output terminal to vary by changing the voltage at the control terminal.

Sakamoto does not teach a variable resister. Fujii teaches an variable resister for the data driver power supply with the input terminal connection to the input power supply and a different variable resister for the scan driver power supply. The terminal connections for the variable resister for the scan power supply, however, do not track the terminal connections of claim 2. Fujii, figure 1.

Nishioka teaches a variable resister 81b having a resistance variation terminal connected to the control terminal of the amplifying element. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the constant current control circuit of Nishioka to the display voltage supply circuit of Fujii and Sakamoto to create a scan driver power circuit. Nishioka points out that "It is an object of the present invention to solve the problems associated with the generation of heat and the rush current during the application of the scan signal while reducing the charging and discharging time." Nishioka, col. 1, lines 54 – 57. Nishioka teaches the advantage of its power circuit for scan driver. "Thus, the constant current control circuit 81 performs control to provide a constant current in response to the control signal at a high level input from the input terminal S1. Nishioka, col. 6, lines 2 – 5.

Claim 8 (amended)

Nishoika teaches a resister 81c having a terminal connected to the input power supply. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. Nishioka teaches a Zener diode 81d having a cathode connected to the resister and an anode to ground. Nishioka, figures 4 and 6 and col. 6, lines 19 – 21.

Claim 14

Bipolar Transistors. Claim 14 is dependant on claim 2 and adds that the amplifying elements are bipolar transistors. Nishioka teaches the use of bipolar transistors in the scan driver and the data driver. Nishioka, col. 8, lines 44 – 48.

Claim 15

Field Effect Transistors. Claim 15 is dependant on claim 2 and adds that the amplifying elements are field effect transistors. Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., and Fujii et al., as applied to claim 1 above, and further in view of The Electrical Engineering Handbook, CRC Press, 1993.

Claim 12

Claim 12 adds that the amplifying elements are MOS transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14.

Sakamoto does not teach that the transistors are MOS transistors and Fujii uses the MOS transistors in a slightly different way in the circuit.

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Sakamoto. The

Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568. A MOS transistor, often labeled a MOS-FET, is a type of field effect transistor.

11. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. and Fujii et al., as applied to claim 1 above, and further in view of Ishizaki, et al., USPN 5,473,289.

Claim 13

Operational Amplifiers. Claim 13 is dependant on claim 1 and adds that the amplifying elements are operational amplifiers.

Sakamoto does not teach the use of operational amplifiers. Fujii teaches operational amplifiers but in a slightly different way than described in claim 13. Fujii, figure 1 and col. 6, lines 31 – 34.

Ishizaki, however, teaches the use of a temperature control circuit 101 having a operational amplifier with the control terminal connected to a plurality of diodes to ground and a resister to the voltage source. Ishizaki, figure 6(b), col. 7, lines 49 – 57.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature control circuit of Ishizaki with the data driver power circuit of Sakamoto. Ishizaki teaches that such a circuit "generates a voltage which is proportion to the detected voltage." Ishizaki, col. 7, lines 29 – 30. See also Ishizaki, col. 8, lines 2 – 7; and

figure 3. One would be motivated to use the Ishizaki circuit because operational amplifiers are readily available and the Ishizaki circuit has a linear output.

Claim 17

Operational Amplifiers. Claim 17 is dependant on claim 2 and adds that the amplifying elements are operational amplifiers.

Sakamoto and Nishioka do not teach the use of operational amplifiers. Fujii teaches operational amplifiers but in a slightly different way than described in claim 13. Fujii, figure 1 and col. 6, lines 31 – 34.

Ishizaki, however, teaches the use of a temperature control circuit 101 having a operational amplifier with the control terminal connected to a plurality of diodes to ground and a resister to the voltage source. Ishizaki, figure 6(b), col. 7, lines 49 – 57.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature control circuit of Ishizaki with the data driver power circuit of Sakamoto. Ishizaki teaches that such a circuit "generates a voltage which is proportion to the detected voltage." Ishizaki, col. 7, lines 29 – 30. See also Ishizaki, col. 8, lines 2 – 7; and figure 3. One would be motivated to use the Ishizaki circuit because operational amplifiers are readily available and the Ishizaki circuit has a linear output.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. and Sakamoto et al., as applied to claim 2 above, and further in view of The Electrical Engineering Handbook.

Claim 16

MOS Transistors. Claim 16 is dependant on claim 2 and adds that the amplifying elements are MOS transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14.

Sakamoto does not teach that the transistors are MOS transistors and Fujii uses the MOS transistors in a slightly different way in the circuit.

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Sakamoto. The Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568.

Response to Arguments

13. Applicant's arguments filed 31 December 2002 have been fully considered but they are not persuasive.

Applicant argues that Fujii in view of Sakamoto does not describe a power supply circuit having a brightness control circuit to change scan driver voltage, a voltage regulation circuit, and a temperature compensation circuit. As to the brightness control circuit, the specification teaches

using a variable resistor 124 to change the scan drive voltage. Specification, page 11, lines 2 – 5 and figure 3B. Fujii teaches using a variable resistor R1 to change the scan drive voltage. Fujii, col. 6, lines 4 – 15; and figure 1. As to the temperature compensation circuit, Sakamoto teaches a temperature compensation circuit. The title of Sakamoto is "D.C. Power Source with Temperature Compensation." Sakamoto states, "A main purpose of the present invention is, therefore, to provide a D.C. power source having a temperature compensation circuit..." Sakamoto, col. 1, lines 29 – 31. As to voltage regulation circuit, neither Fujii nor Sakamoto specifically uses the term "voltage regulation circuit." As claims 2 and 3 makes clear, however, "the voltage regulation circuit and the temperature compensation circuit comprise a diode group having a plurality of series connected diodes connected between the control terminal of the amplifying element and ground." This is the power supply circuit described in the specification and the power supply circuit described in Sakamoto. Sakamoto, figure 2; col. 3, lines 7 - 13. Applicant desires to claim the circuit shown as figure 3A in the specification, a circuit nearly identical to the circuit show by Sakamoto's figure 2. So far, applicant has present few claims that distinguish applicant's invention over Fujii in view of Sakamoto or even over the admitted prior art shown in the specification as figure 1.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600